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10/721,331	11/26/2003	Kenji Wada	109802.01	8385

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/721,331	WADA, KENJI
	Examiner	Art Unit
	Heather A. Doty	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/891,407.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 10 is objected to because of the following informalities: In lines 3 and 4 of claim 10, the word "second" should be omitted because in claim 5 there is no mention of a first dielectric film. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 5–7 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoshi et al. (U.S. 6,252,266).

With respect to claim 5, Hoshi et al. teaches a method to manufacture a semiconductor device, comprising preparing a semiconductor wafer including a plurality of semiconductor chip forming sections, each having an electrode (column 16, claims 10 and 11); forming a first hole in the electrode (**42**a in Figs. 11-12; column 8, lines 42-46); forming a second hole penetrating the semiconductor wafer (**43**a in Figs. 11-12; column 8, lines 42-46), the second through hole communicating (electrically through the electrode) with the first through hole; and forming a conduction layer (**50** in Fig. 12; column 8, lines 54-57) that extends via the first and second through holes from a first

surface of each of the semiconductor chip forming sections on which the electrode is formed to a second surface opposite to the first surface, the conduction layer being electrically connected to the electrode (Fig. 12; column 8, lines 54-57).

With respect to claim 6, Hoshi et al. teaches the method to manufacture a semiconductor device according to claim 5, as noted above, the second through hole having a straight internal wall, as shown in Fig. 12.

With respect to claim 7, Hoshi et al. teaches the method to manufacture a semiconductor device according to claim 5, as noted above, a first size of the first through hole being the same as a second size of the second through hole, as shown in Fig. 12.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (U.S. 6,252,266) in view of Konishi et al. (U.S. 4,016,593).

Hoshi et al. teaches the method to manufacture a semiconductor device according to claim 5 (note 35 U.S.C. 102(e) rejection above), but does not teach a first size of the first through hole being greater than a second size of a second through hole.

Konishi et al. teaches a semiconductor device comprising a first through hole in an electrode (**52** in Fig. 6) and a second through hole in the semiconductor wafer (**519**

in Fig. 6), wherein the first size of the first through hole is greater than the second size of the second through hole.

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to form a semiconductor device according to the method recited in claim 5, as taught by Hoshi et al., wherein the first through hole is larger than the second through hole, as taught by Konishi et al. The motivation for doing so at the time of the invention would have been to allow light to enter the second hole without reflecting off of the electrode, as shown in Fig. 6 of Konishi, et al.

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (U.S. 6,252,266) in view of Birdsley et al. (U.S. 6,720,641).

With respect to claim 9, Hoshi et al. teaches the method to manufacture a semiconductor device according to claim 5 (note35 U.S.C. 102(e) rejection above), but does not teach forming a dielectric film covering the electrode and an interior of the first through hole; forming a third through hold penetrating the first dielectric film, the third through hole exposing the electrode, the conduction layer being electrically connected to the electrode via the third through hole.

Birdsley et al. teaches a method to manufacture a semiconductor device comprising the steps of forming through holes penetrating the semiconductor wafer, forming a dielectric film covering the interior of the through holes (**146** in Fig. 2), forming holes penetrating the dielectric film, and forming conductive layers (**140** in Fig. 2) within the holes in the dielectric layer.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hoshi et al. and Birdsley et al. to manufacture a semiconductor device according to the method steps of claim 5, as taught by Hoshi et al., deposit a dielectric film over the wafer including the electrode and into the through hole, as taught by Birdsley et al., form a third hole penetrating the first dielectric film, as taught by Birdsley et al., to expose the electrode, and deposit conductive material within the third hole, as taught by Birdsley et al., which will connect to the electrode via the third hole. The motivation for doing so at the time of the invention would have been to electrically insulate the conduction layer from the substrate, as expressly taught by Birdsley et al. (column 5, lines 16-17).

With respect to claim 10, Hoshi et al. teaches the method according to claim 5 (note 35 U.S.C. 102(e) rejection above), but does not teach forming a dielectric film on an internal wall surface of the second through hole, the conduction layer being formed on the dielectric film.

Birdsley et al. teaches forming a dielectric film on an internal wall surface of a through hole in a semiconductor through hole, and forming a conduction layer on the dielectric film (Fig. 2).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hoshi et al. and Birdsley et al. to manufacture a semiconductor device according to claim 5, as taught by Hoshi et al., and form a dielectric film on an internal wall of the through hole in the semiconductor wafer and form a conduction layer on the dielectric film, as taught by Birdsley et al. The

motivation for doing so at the time of the invention would have been to electrically insulate the conduction layer from the substrate, as noted above and expressly taught by Birdsley et al. (column 5, lines 16-17).

With respect to claim 11, Hoshi et al. teaches a method to manufacture a semiconductor device, comprising preparing a semiconductor wafer including a plurality of semiconductor chip forming sections, each having an electrode (column 16, claims 10 and 11); forming a first hole in the electrode (hole through the electrode, **42**a in Figs. 11-12; column 8, lines 42-46); forming a second hole penetrating the semiconductor wafer (hole through the wafer, **42**a in Figs. 11-12; column 8, lines 42-46), the second through hole communicating with the first through hole; and forming a conduction layer (**50** in Fig. 12; column 8, lines 54-57) that extends via the first and second through holes from a first surface of each of the semiconductor chip forming sections on which the electrode is formed to a second surface opposite to the first surface, the conduction layer being electrically connected to the electrode (Fig. 12; column 8, lines 54-57).

Hoshi et al. does not teach forming a first dielectric film covering the electrode and an interior of the first through hole; forming a second dielectric film on an internal wall surface of the second through hole; forming an opening penetrating the first and second dielectric films, the opening exposing the electrode, the conduction layer being electrically connected to the electrode via the opening.

Birdsley et al. teaches a method to manufacture a semiconductor device comprising the steps of forming through holes penetrating the semiconductor wafer, forming a dielectric film covering the interior of the through holes (**146** in Fig. 2), forming

holes penetrating the dielectric film, and forming conductive layers (**140** in Fig. 2) within the holes in the dielectric layer.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hoshi et al. and Birdsley et al. to manufacture a semiconductor device according to the method steps of claim 5, as taught by Hoshi et al., deposit a dielectric film over the wafer including the electrode and into the first and second connected through holes, as taught by Birdsley et al., form a third hole penetrating the dielectric film on the first and second connected through holes, as taught by Birdsley et al., to expose the electrode, and deposit conductive material within the third hole, as taught by Birdsley et al., which will connect to the electrode via the third hole. The motivation for doing so at the time of the invention would have been to electrically insulate the conduction layer from the substrate, as noted above and expressly taught by Birdsley et al. (column 5, lines 16-17).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (U.S. 6,252,266) in view of Tseng (U.S. 5,843,821).

Hoshi et al. teaches the method to manufacture a semiconductor device according to claim 5 (note 35 U.S.C. 102(e) rejection above), but does not teach the first through hole being formed by a dry etching.

Tseng teaches a method to manufacture a semiconductor device including the step of dry etching a hole in an electrode (column 6, lines 11-21).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hoshi et al. and Tseng to

manufacture a semiconductor device by forming a through hole in an electrode, as taught by Hoshi et all, wherein the through hole is formed with a dry etch process, as taught by Tseng. The motivation for doing so at the time of the invention would have been to achieve an anisotropic etch, as taught by Tseng (column 6, line 12).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (U.S. 6,252,266) in view of Dhong et al. (U.S. 6,221,769) and Wolf et al. (*Silicon Processing for the VLSI Era*, v. 1, 2nd edition).

Hoshi et al. teaches the method to manufacture a semiconductor device according to claim 5 (note 35 U.S.C. 102(e) rejection above), but does not teach the conduction layer being formed by the plating method.

Dhong et al. teaches a method to manufacture a semiconductor device comprising the step of forming a conduction layer that extends through multiple via holes from the first surface of a semiconductor chip to a second, opposite surface, by the plating method (Fig. 2; column 6, lines 25-28).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form the conduction layer taught by Hoshi et al. by the plating method, as taught by Dhong et al. The motivation for doing so at the time of the invention would have been because metal plating offers high throughput and therefore low costs, as taught by Wolf et al. (pg. 784, second full paragraph).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER